• Features

- Used with the DC003, DC004, DC005, and DC010 to implement a direct memory access interface.
- Contains two 8-bit binary up counters for word byte count and bus address.
- Implements low-power Schottky circuits.
- Includes read and write control logic.
- Includes comparison circuit for device address selection.
- Two DC006s can be cascaded for 16-bit register implementation.
- Contains internal 8-line bus and three-state bus drivers.

• Description

The DC006 word count/bus address logic, contained in a 20-pin dual-inline (DIP) package, is designed for use in a direct memory access (DMA) device interface. The DC006 is a low-power Schottky device that connects to the three-state outputs of the DC005 transceiver. The DC006 is controlled by the DC004 register selector, the DC010 direct memory access, and ancillary logic. Figure 1 is a simplified block diagram of the DC006.

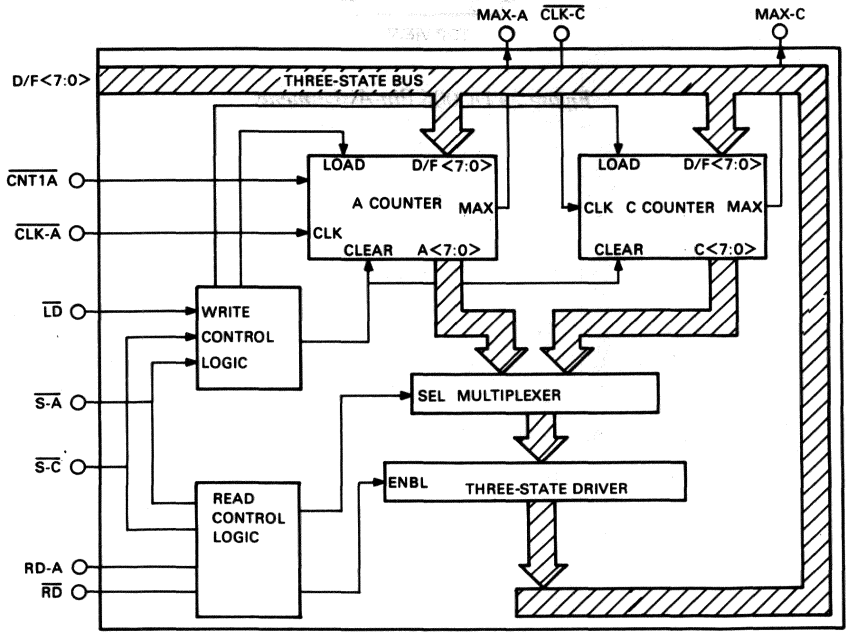


Figure 1 • DC006 Simplified Block Diagram

It includes two separately controlled 8-bit binary up-counters, one for word (byte) count and one for bus address. Each counter can be separately loaded and cleared. The word counter (C counter) is incremented by a count of one and the address counter (A counter) is incremented by a count of one for byte addressing and by a count of two for word addressing. Each counter is read separately. Data from the DC006 is transferred to the three-state bus through the internal drivers.

• Pin and Signal Descriptions

This section provides a brief description of the input and output signals and power and ground connections of the DC005 20-pin DIP. The pin assignments are identified in Figure 2 and then summarized in Table 1.

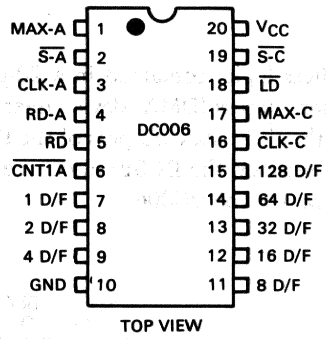


Figure 2 • DC006 Pin Assignments

Table 1 • DC006 Pin and Signal Summary

Pin	Signal	Input/Output	Definition/Function
6	$\overline{\text{CNT1A}}$	input	Increment counter A—Controls the least significant bit of the A counter . When low the A counter is incremented by one. When high, the least-significant bit of the A counter is disabled and the count is incremented by two. When two counters are cascaded, this input should be connected to ground.
3	$\overline{\text{CLK-A}}$	input	Clock A counter—The negative edge of this signal increments the A counter by one or two counts depending on the $\overline{\text{CNT1A}}$ level. The $\overline{\text{CNT1A}}$ and $\overline{\text{LD}}$ signals must be stable while the $\overline{\text{CLK-A}}$ signal is high.
16	$\overline{\text{CLK-C}}$	input	Clock C counter—The negative edge of this signal increments the C counter by a count of one. The $\overline{\text{LD}}$ signal must be stable while the $\overline{\text{CLK-C}}$ signal is high.
2	$\overline{\text{S-A}}$	input	Select A counter—Selects the outputs and functions of the A counter during read and write operations as specified in Tables 2 and 3.
19	$\overline{\text{S-C}}$	input	Select C counter—Selects the outputs and functions of the C counter during read and write operations as specified in Tables 2 and 3.
4	RD-A	input	Read A counter—Selects the outputs and functions of the A counter during read and write operations as specified in Tables 2 and 3.
5	$\overline{\text{RD}}$	input	Read—Enables a read operation as specified in Tables 2 and 3.
18	$\overline{\text{LD}}$	input	Load—A high-to-low transition of this signal enables a load operation to be performed as specified in Table 3. When $\overline{\text{LD}}$ is low, data changes will not occur.
7 8 9 11 12 13 14 15	1D/F 2D/F 4D/F 8D/F 16D/F 32D/F 64D/F 128D/F	outputs*	Data bus—Eight bidirectional lines used to transfer data into or out of the A counter or C counter.
1	MAX-A	output	Maximum A count—Indicates that the A counter has reached a maximum count. The maximum count is 376 when counting by two and 377 when counting by one. The signal is generated by gating $\overline{\text{CLK-A}}$ and the maximum count condition of the counter.

Pin	Signal	Input/Output	Definition/Function
17	MAX-C	output	Maximum C count—Indicates that the C counter has reached a maximum count of 377. This signal is generated by gating $\overline{\text{CLK-C}}$ and the maximum count condition.
20	V_{CC}	input	Voltage—Power supply dc voltage
10	GND	input	Ground—Common ground connection

*TTL three-state

Functional Description

Figure 3 is a simplified logic diagram of the DC006 that shows the read and write control logic, the inputs and outputs of the A and C counters, and the multiplexer logic. Table 2 lists the read and select inputs required to read the counter outputs. Table 3 lists the write-control inputs required to load and clear the counters.

Table 2 • DC006 Read-control Functions

Input Levels*				Output Functions
RD-A	$\overline{\text{RD}}$	$\overline{\text{S-A}}$	$\overline{\text{S-C}}$	D/F<7:0>
L	L	L	L	Clear A and C counters, read C counter
L	L	L	H	A<7:0>
L	L	H	H	C<7:0>
L	H	H	H	High-impedance
L	H	X	X	High-impedance
H	L	L	L	Clear A and C counters, read A counter
H	L	L	H	A<7:0>
H	L	H	L	A<7:0>
H	L	H	H	A<7:0>
H	H	L	L	Clear A and C counters, read A counter
H	H	L	H	A<7:0>
H	H	H	L	A<7:0>
H	H	H	H	A<7:0>

*L = TTL low, H = TTL high, X = TTL low or high

Table 3 • DC006 Write-control Functions

Inputs Levels[1]					Function
RD-A	$\overline{RD}$	$\overline{LD}$	$\overline{S\text{-}A}$	$\overline{S\text{-}C}$	
L	H	H-L	L	L	Illegal[2]
		H-L	L	H	Load A<7:0>
		H-L	H	L	Load A<7:0>
		X	H	H	Word count/Bus address not selected
		H	L	L	Clear A and B counters
		H	L	H	Loading disabled
		H	H	L	Loading disabled

[1]L = TTL low, H = TTL high, X = TTL low or high, H-L = high-to-low transition.
[2]Simultaneous load and clear operation results in a clear.

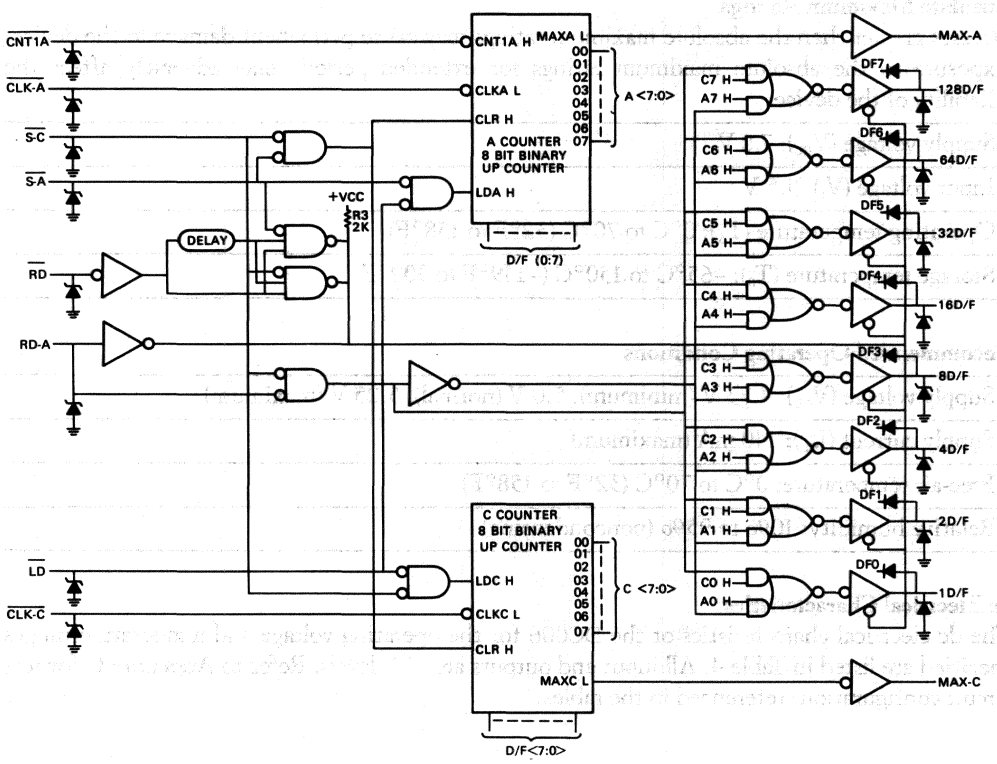


Figure 3 • DC006 Simplified Logic Diagram

• Application Information

Refer to the *Chipkit Users Manual LSI-11 Bus Interface Chips* (document no. EJ-01387-92) for general application information. The Q-bus is an LSI-11 bus.

• Specifications

The mechanical, electrical, and environmental characteristics and specifications for the DC005 are described in the following paragraphs. The test conditions for the electrical values are as follows unless specified otherwise.

- Operating temperature (T_A): 0°C to 70°C
- Supply voltage (V_{CC}): 5.0 V ±5%

Mechanical Configuration

The physical dimensions of the DC005 20-pin DIP are contained in Appendix E. The materials and construction of the molded DIP are defined in Digital Specification A-PS-1900002-GS.

Absolute Maximum Ratings

Stresses greater than the absolute maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum ratings for extended periods may adversely affect the reliability of the device.

- Supply voltage (V_{CC}): 7.0 V
- Input voltage (V_I): 5.5 V
- Operating temperature (T_A): 0°C to 70°C (32°F to 158°F)
- Storage temperature (T_S): –65°C to 150°C (–149°F to 302°F)

Recommended Operating Conditions

- Supply voltage (V_{CC}): 4.75 V (minimum), 5.0 V (normal), 5.25 V (maximum)
- Supply current (I_{CC}): 140 mA (maximum)
- Free-air temperature: 0°C to 70°C (32°F to 158°F)
- Relative humidity: 10% to 95% (noncondensing)

dc Electrical Characteristics

The dc electrical characteristics of the DC006 for the operating voltage and temperature ranges specified are listed in Table 4. All input and outputs are TTL levels. Refer to Appendix C for test circuit configurations referenced in the tables.

Table 4 • DC006 TTL Input and Output Parameters (nonbus)

Parameter	Symbol	Test Condition	Requirements Min.	Max.	Units	Test Circuit
High-level input voltage	V_{IH}		2.0	—	V	C1,C2
Low-level input voltage	V_{IL}		—	0.8	V	C1,C2
Input clamp voltage	V_I	V_{CC}=4.75 V I_I=−18 mA	—	−1.2	V	C3
High-level output voltage	V_{OH}	V_{CC}=4.75 I_O=−1.0 mA	2.7	—	V	C1
Low-level output voltage	V_{OL}	V_{CC}=4.75 V I_O=20 mA	—	0.5	V	C2
Input current at maximum input voltage	I_I	V_{CC}=5.25 V V_I=5.5 V[1]	—	1.0	mA	C4
High-level input current	I_{IH}	V_{CC}=5.25 V V_I=2.7 V				C4
Three-state			—	50	µA	
Not three-state			—	55	µA	
Low-level input current	I_{IL}	V_{CC}=5.25 V V_I=0.5 V				C5
$\overline{\text{CLK-A}}$, $\overline{\text{CLK-C}}$			—	−1.1	mA	
$\overline{\text{CNT1A}}$			—	−1.7	mA	
D/F<0:7> $\overline{\text{LD}}$, $\overline{\text{RD}}$, $\overline{\text{S-C}}$, $\overline{\text{S-A}}$			—	100	µA	
RD-A			—	200	µA	
High-impedance output current	I_O[1]	V_{CC}=5.25 V V_O=3.75 V	—	100	µA	C1
Short-circuit output current	I_{OS}	V_{CC}=5.25 V[2]	−40	−100	mA	C6
Supply current	I_{CC}	V_{CC}=5.25 V	—	170	mA	C7

[1]Three-state TTL output in off state.

[2]Not more than one output shall be short circuited at a time and the duration of the short must not exceed 1 second.

ac Electrical Characteristics

The input and output signal timing for the DC006 is shown in Figure 4. Table 5 lists the setup time and pulse characteristics for the times specified in Figure 4. Table 6 lists the propagation delays for the signal timing references in Figure 4. Refer to Appendix D for the standard input and output voltage waveforms parameters used to measure propagation delay. The output loading circuit for the open collectors and the three-state output loading circuit and voltage waveforms are shown in Figure 5. These circuits are referenced in Table 6.

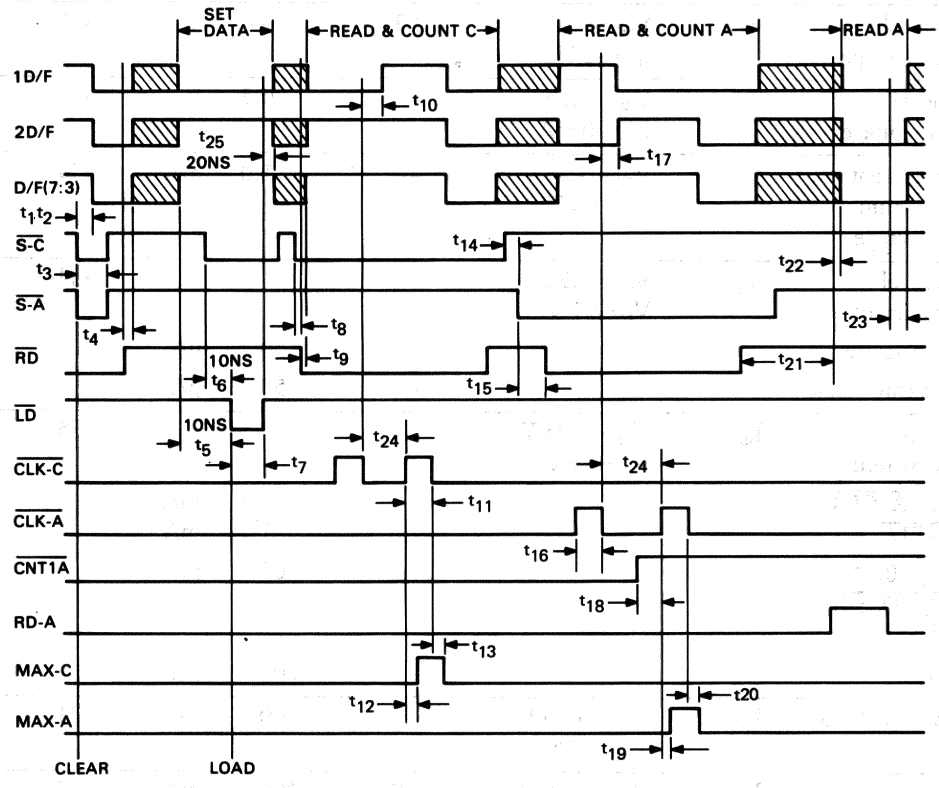


Figure 4 • DC006 Signal Timing Sequence

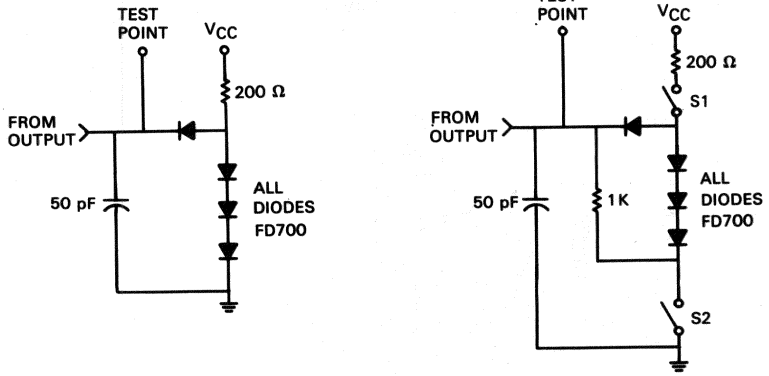
Table 5 • DC006 Pulse-width and Setup time

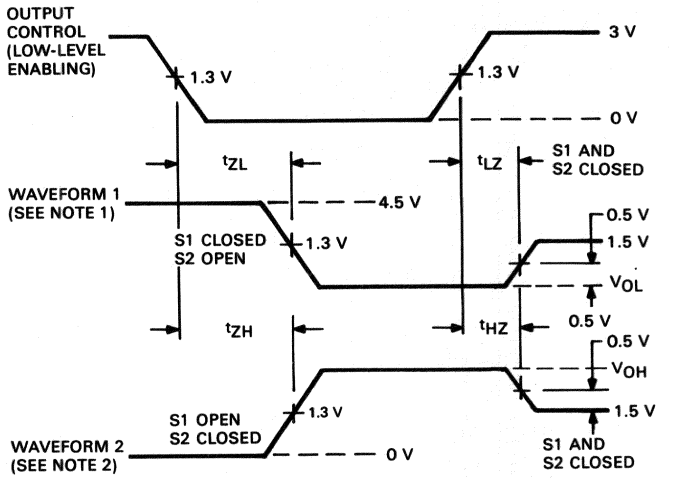
Time Reference	Signals Reference	Minimum Duration (ns)
t_3 (pulse width)	$\overline{\text{S-C}}$ to $\overline{\text{S-A}}$	50
t_5 (setup)	D/F<7:0> H to $\overline{\text{LD}}$	10
t_6 (setup)	$\overline{\text{S-C}}$ to $\overline{\text{LD}}$	10
t_7 (pulse width)	$\overline{\text{LD}}$	90
t_8 (setup)	$\overline{\text{S-C}}$ to RD	20
t_{11} (pulse width)	$\overline{\text{CLK-C}}$	40
t_{14} (setup)	S-C to S-A	20
t_{15} (setup)	S-A to RD	10
t_{16} (pulse width)	$\overline{\text{CLK-A}}$	40
t_{18} (setup)	$\overline{\text{CNT1A}}$ to $\overline{\text{CLK-A}}$	45
t_{21} (setup)	$\overline{\text{RD}}$ to RD-A	15
t_{24} (off)	$\overline{\text{CLK-A}}$, $\overline{\text{CLK-C}}$	40
t_{25} (data hold)	$\overline{\text{LD}}$ to data in 20	20

Table 6 • DC006 Signal Propagation Delay

Timing Reference	Input Signal (Transition)	Output Signal (Transition)*	Test Condition	Propagation Delay (ns) Min.	Max.
t_1	$\overline{\text{S-C}}$ (H-L) $\overline{\text{S-A}}$ (H-L)	D/F<7:0> (X-L)	Load A RD-A = 0.4 V (C counter)	15	80
t_2	$\overline{\text{S-C}}$ (H-L) $\overline{\text{S-A}}$ (H-L)	D/F<7:0> (X-L)	Load A RD-A = 0.4 V (A counter)	15	80
t_4	$\overline{\text{RD}}$ (L-H)	D/F<7:0>-(Z)	Load A	10	30
t_9	$\overline{\text{RD}}$ (H-L)	(Z)-D/F<7:0>	Load A	34	80
t_{10}	$\overline{\text{CLK-C}}$ (H-L)	MAX-C (L-H)	Load A	18	55
t_{12}	$\overline{\text{CLK-C}}$ (L-H)	MAX-C (L-H)	Load B	10	35
t_{19}	$\overline{\text{CLK-A}}$ (L-H)	MAX-A (L-H)	Load B	10	35
t_{13}	$\overline{\text{CLK-C}}$ (H-L)	MAX-C (L-H)	Load B	10	35
t_{17}	$\overline{\text{CLK-A}}$ (H-L)	D/F2 (L-H)	Load A	18	55
t_{20}	$\overline{\text{CLK-A}}$ (H-L)	MAX-A (H-L)	Load B	10	35
t_{22}	RD-A (L-H)	D/F<7:0> (Z-L) (Z-H)	Load A Load A	10 10	30 30
t_{23}	RD-A (H-L)	D/F<7:0> (L-Z) (H-Z)	Load A Load A	8 8	25 25

*Z = high impedance





NOTE

1 WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW EXCEPT WHEN DISABLED BY THE OUTPUT CONTROL.

2 WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH EXCEPT WHEN DISABLED BY OUTPUT CONTROL

Figure 5 ▪ DC003 Output Load Circuits